High density
High layer count

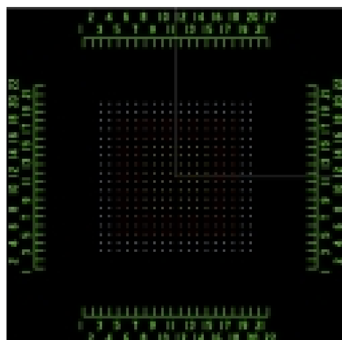
ビルドアップ基板以上の高密度配線を一般多層工法で実現！

High density wiring exceeding the level of build-up process board is realized by conventional multi layer process!

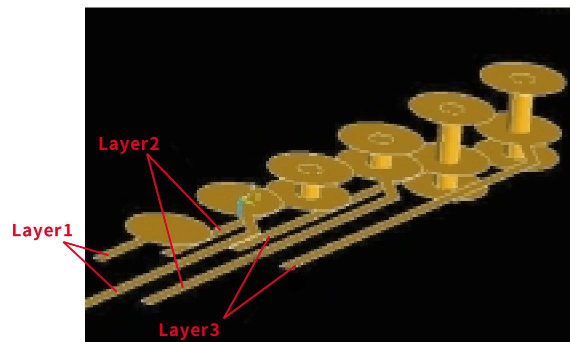
Multi SVH工法による0.5mmピッチ配線基板

0.5mm pitch wiring board by Multi SVH process

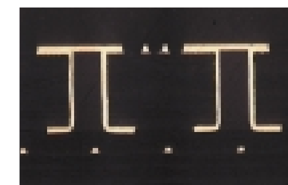
ピンレイアウト(例) Pin layout (example)



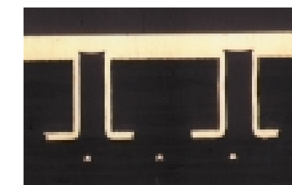
配線モデル Wiring model



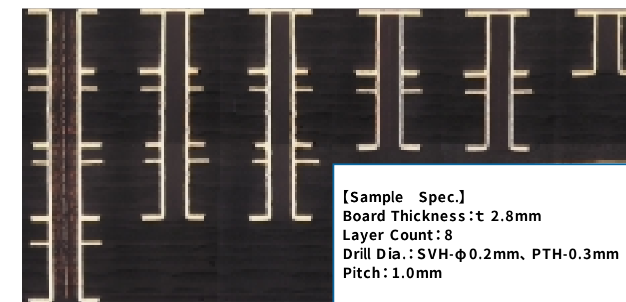
表層めっき厚比較 Comparison of surface plating thickness



New process (X-Section)



Conventional process



【Sample Spec.】
Board Thickness：t 2.8mm
Layer Count：8
Drill Dia.：SVH-φ0.2mm、PTH-0.3mm
Pitch：1.0mm

New process (Y-Section)

SVH 3段形成後の外層 導体厚を40μmに コントロール

Outer conductor layer thickness after fabrication of 3 levels SVH is controlled to 40μm.

SVHの下層を配線エリアとして有効活用

Lower layer of SVH is effectively used as the wiring area.

外層Line/Space =70/70μm

Outer layer Line/Space =70/70μm

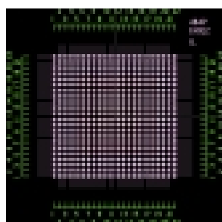
特長 Features

- 22×22列のフルマトリクス配線を6層の信号層で実現。
- SVHは最小φ0.1mmの小径を採用。
- SVHは多段形成が可能。
  （Ex：Lay.1～Lay.2　Lay.1～Lay.4　Lay.1～Lay.6の3段）
- コンベンショナル工法を採用し機械強度やリペア耐性を維持。
- 最終の外層導体厚を40μm前後にコントロールすることで、高精細回路の形成が可能。
- 高多層（36層）/高板厚（6.2t）/大型（φ440）に対応。
- 貫通スルーホールとの併用が可能。

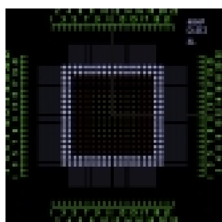
- 22x22 rows full matrix wiring is realized by 6 signal layers.
- Small diameter of minimum φ0.1mm is employed for SVH.
- SVH can be fabricated in multiple levels.
  (Example: 3 levels consisting of Lay. 1～Lay. 2, Lay. 1～Lay. 4 and Lay. 1～Lay. 6)
- Mechanical strength and repairability are maintained by employment of the conventional process.
- Fine pitch circuit can be fabricated by controlling the final outer conductor layer thickness to approximately 40μm.
- High layer count (36 layers), high board thickness (6.2t) and large size (φ440) are realized.
- Coexistence with complete through holes is possible.

配線例 Wiring examples

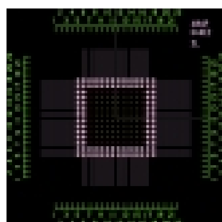
Layer1(2 row wiring)



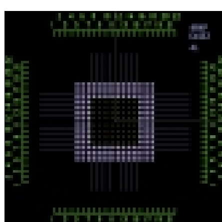
Layer2(2 row wiring)



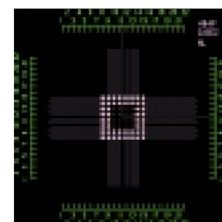
Layer3(2 row wiring)



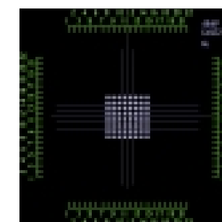
Layer4(1row wiring)



Layer5(2 row wiring)



Layer6(2 row wiring)



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